***ECE457 Digital IC Design***

***Project #3 Due 11/13/19***

**Perform the following Project:**

1. Design of 16-to-1 Multiplexer (MUX) using both of (1) only transmission gates (TG) and (2) other conventional CMOS gates. Compare the TG design with conventional CMOS gate designs by performance, power, chip size, number of transistors, etc.

For a report, put the following as a guide for your own design:

1. Draw logic symbol, schematic for simulation.
2. Draw stick diagram and Euler’s paths
3. Electric Layout and IRSIM
4. LT SPICE where needed to show performance
5. Verify your design by putting pulses to see the outputs.
6. Complete a Truth table for the MUX.
7. Find a Boolean expression for the MUX.
8. Extract Rp, Rn, and C's from your layout using electric. Use the extraction guide I put under the CAD folder.
9. Run LTSPICE in Electric to "plot" waveforms of Vinputs and Vout. Use 100ns period, rise time (tr) and fall time (tf) as 5ns for Vin. Use 50% duty cycle which means 50% logic high and 50% logic low levels.

This is a hint for LTSPICE: For the parasitic extraction, follow exactly what it says in this link: <http://cmosedu.com/cmos1/ltspice/ltspice_electric.htm>. In the drop-down menu labeled "Parasitics", select the "Conservative RC" option instead of the default "Trans area/Perim only" option. This is what gives you the R and C values when you click Tools -> Simulation (Spice) -> Write Spice Deck. In the tutorial it tells you to save the file [C5\_models.txt](http://cmosedu.com/videos/electric/tutorial2/C5_models.txt) to C:\Electric for SPICE simulations. Then in the LTSPICE code you have to write ".include C:\Electric\C5\_models.txt".

1. Measure the output waveform by taking measurements for tr, tf, TLH and THL for the first input, *W0*.
2. Write some paragraphs for design and measurements and make a project report. Write Figure numbers and captions. Attach the cover page.

**What to turn-in:**

1. **You will be graded for points in the table of the cover sheet.**
2. **Use single space with 12 pt font. Do not double space due to page counts.**
3. **Do not try to make your report long with unnecessary pages that includes non-trivial data such as printing extraction data.**
4. A typed report that has the following:
   1. Cover page (print the attached cover page)
   2. Executive Summary: Summarize your project in 1/2 –page format. **Note: Single space format.**
   3. Introduction: Provide some background and motivation
   4. Approach and calculations: Put schematics and details of the design. Put detailed calculations of all parameters. Put theory of the operation and others. Use schematic or drawing tools to draw schematic.
   5. LTSPICE Simulations: Put the output of the circuit in piece by piece as you need to analyze. Put input and output waveforms on the same panel.
   6. Perform waveform measurements for rise/fall times and periods.
   7. Provide transistor counts, power, chip size, trade-offs, etc.
   8. Conclusion: Put what you observed and what you did.
   9. **References**: put any papers that are relevant to this project by using the IEEE format and reference in your text.
5. Calculate the following parameters:
   1. Calculate transistor sizes (W/L) and delays.
   2. Power dissipation of the device. Use hand calculation after the extraction and let LTSpice provide the supply current for power.
   3. Total chip area. Provide in units of micrometer square.
6. Turn in your project on Blackboard.
7. ***Five points will be deducted for not following the directions.***

EE457: Digital IC Design

Fall Semester 2019

Project 3 Report Cover Sheet

Due 11/13/2019

## **PROJECT TITLE: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**

Student Name:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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| Put Check for completion | Topics | GRADES |
|  | Section1: Executive Summary | /5 |
|  | Section 2: Introduction and Background | /5 |
|  | Section 3: Electric Circuit Schematics | /10 |
|  | Section 4: Detailed Electric Layouts | /25 |
|  | Section 5: IRSIM Logic Simulations and Measurements for Layout and Schematic (must provide comparisons between the two) | /10 |
|  | Section 6: LTSPICE code and parasitic extractions with calculation analysis for charge sharing. Put only samples of code. | /15 |
|  | Section 7: Measurements in LTSPICE for delays for Layout and Schematic (must provide comparisons between the two) | /15 |
|  | Section 8: Measurements of power, delay, chip area, timing, number of transistors for the layout. | Power /2  Delay /2  Area /2  #tran /4 |
|  | Section 9: Conclusion and References | /5 |
|  | Penalty |  |
|  | TOTAL | **/100** |